

I Claim:

1. A method of performing single bit error corrected M-bit words that have been scrambled using a self synchronizing scrambler, the method comprising the  
5 steps of:
  - a) calculating an N-bit CRC every K words of a block of J words using a generator polynomial, where J is a non-zero integer multiple of K;
  - b) forming an M-bit word from the calculated N-bit CRCs, where M is a non-zero  
10 integer multiple of N, and appending this word to the block of J words to form a block of J+1 words for transmission;
  - c) calculating, responsive to receiving a block of J+1 words, another N-bit CRC every K words of the first J words of the received block of J+1 words and using,  
15 from the appended word, the N-bit CRC corresponding to the K words in each calculation; and
  - d) correcting, responsive to one of the another N-bit CRCs, computed at the receiver, having a non-zero value, an errored bit in the received block of J+1  
20 words, the errored bit being indicated by an entry in a table indexed according to the non-zero value.
2. The method as defined in claim 1 wherein the M-bit words are 64b/66b encoded words (M=64 bits).  
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3. The method as defined in claim 2 wherein the N-bit CRC is a 16bit CRC.
4. The method as defined in claim 3 wherein K=2 and J=8.

5. The method as defined in claim 1 wherein the generator polynomial is  $x^{16}+x^{12}+x^5+1$ .

6. An error control block receiver (ECB\_Rx) for receiving and performing  
5 single bit error corrected M-bit words that have been scrambled using a self synchronizing scrambler comprising:

synchronizing means to synchronize the error control block;

a buffer to store the M-bit words in a tabular buffer;

CRC 16 computation means to calculate a syndrome; and

10 a syndrome table, the calculated syndrome being compared with the syndrome table to detect a single bit error.

7. The ECB\_Rx as defined in claim 6 wherein the M-bit words are 64b/66b encoded words.

15 8. The ECB\_Rx as defined in claim 7 wherein the tabular buffer is a 9x8 byte buffer.

9. An error control block transmitter (ECB\_Tx) for use in a single bit error  
20 corrected M-bit encoded words, the ECB\_Tx comprising computation means to calculate CRC 16 of code words;

a buffer to store the code words in a tabular buffer; and

transmitting means to selectively transmit the code words.

25 10. The ECB\_Tx as defined in claim 9 wherein the M-bit encoded words are 64b/66b encoded words.

11. The ECB\_Tx as defined in claim 10 wherein the tabular buffer is a 9x8 byte buffer.

12. The ECB\_Tx as defined in claim 9 wherein the computation means uses the generator polynomial  $x^{16}+x^{12}+x^5+1$ .

13. The ECB\_Rx as defined in claim 6 wherein the syndrome table is  
5 generated to identify duplicate errors in the M-bit words employing an N-bit CRC calculation.